InP-Based Generic Foundry Platform for Photonic Integrated Circuits

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(Invited Paper)

***Abstract*—The standardization of photonic integration processes for InP has led to versatile and easily accessible generic integration platforms. The generic integration platforms enable the realization of a broad range of applications and lead to a dramatic cost reduction in the development costs of photonic integrated circuits (PICs). This paper addresses the SMART Photonics generic integration platform developments. The integration technology based on butt joint active-passive epitaxy is shown to achieve a platform without compromising the performance of the different components. The individual components or building blocks are described. A process design kit is established with a comprehensive dataset of simulation and layout information for the building blocks. Latest results on process development and optimization are demonstrated. A big step forward is achieved by applying high-resolution ArF lithography, which leads to increased performance for AWGs and a large increase in reproducibility and yield. The generic nature of the platform is demonstrated by analyzing a number of commercial multiproject wafer runs. It is clear that a large variety of applications is addressed with more than 200 designs from industry as well as academia. A number of examples of PICs are displayed to support this. Finally, the design flow is explained, with focus on layout-aware schematic-driven design flow that is required for complex circuits. It can be concluded that generic integration on InP is maturing fast and with the current developments and infrastructure it is the technology of choice for low cost, densely integrated PICs, ready for high-volume manufacturing.**

***Index Terms*—Photonic integrated circuits, microwave photonics, silicon photonics, semiconductor optical amplifiers, quantum well lasers, photodiodes, III-V semiconductor materials.**

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I. Introduction

InP BASED photonic components are mature and reliable sources for communication systems and are deployed in the field for some time. The increasing need for bandwidth is demanding densely integrated photonic circuits and InP is the material of choice for monolithic integration of active and passive components. This allows a scalable solution for large channel numbers without requiring additional high-precision assembly techniques [1], [2]. The technology allows freedom in the placement of amplifiers and lasers in the circuit, ultra high performance modulators [3] and wide band photodetectors (C and L band). Next to this, InP has a number of additional advantages over other integration platforms: because of the integration of sources and detectors, full circuits can be tested on-wafer, the current fab capacity and supply is line with the demand for PICs, this makes InP a low-cost solution for these requirements.

With the introduction of generic integration platforms, the technology has received a large boost. Generic photonic integration [4] adapts the model of micro-electronics in which a large variety of circuits can be made with a limited set of predefined building blocks, fabricated using the same integration process. In photonics, these basic building blocks are waveguides, amplifiers, detectors, phase modulators, that can be integrated into more complex sub circuits.

Generic integration has a number of advantages. By using standardized industrial integration processes, a stable and reproducible performance is achieved. Because the building blocks are predefined, circuit design can be on functional level, leading to a more efficient design flow. The availability of Process Design Kits (PDKs) and design software enables fast and accurate design. The standardized process allows users to share costs in Multi-project wafer (MPW) runs for fast and cost efficient prototyping. Using the MPWs, PICs can be developed and produced much quicker and at lower cost. Because of the much lower design costs, many more businesses will now have the opportunity to design their own chips. Moreover, once the design has been approved, the transition to volume production can take place more efficiently as the process is stable and at

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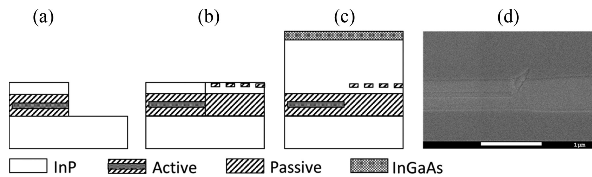

Fig. 1. Overview of the butt-joint process (a) active layer growth and etch, (b) passive layer regrowth and grating patterning, (c) common top cladding growth, (d) SEM image of the resulting butt joint.

an industrial level with a the reliability and yield data readily available.

Researchers at TU Eindhoven have been pioneering generic photonic integration technology since the beginning of the century. In cooperation with a number of partners the generic integration technology has reached maturity [4]. The model has proven successful and InP based integration technology is currently commercially offered by two foundries, brokered by JePPIX [5].

This paper explains in Section II the current state of the art of the generic integration platform as well as the improvements made. This section describes the process technology used for the platform, including an overview of the available building blocks. Finally the introduction of high resolution lithography for enhanced performance of the platform is introduced.

Section III analyses the usage of Multi Project Wafer runs. Furthermore some examples of PICs produced in MPW runs are explained to prove the wide uptake from a variety of users and to demonstrate the versatile nature of the generic process.

The integral design flow is explained in Section IV.

II. Technology and Building Blocks

This section describes the integration process concept and the building blocks that are currently available. Furthermore the development of the building blocks and enhancements to the platform are shown.

A. Integration Process

A key aspect of this integration platform is the use of butt-joint technology, this allows the combination of different material properties without compromising the performance. This technology allows independent optimization of the performance of the active and passive parts on the wafer. In this way e.g. Multi Quantum Well (MQW) gain material, optimized for high gain, can be integrated with bulk InGaAsP passive waveguides for low loss waveguides. Fig. 1 displays a schematic representation of the integration technology, which is explained hereafter.

First the active layer is grown using Metal Organic Chemical Vapor Deposition (MOCVD). For the current MPW transmitter platform, the active layer consists of 4 Quantum Wells (QW) with an emission wavelength at 1550 nm. On this base wafer, active islands are patterned where either lasers, amplifiers or absorbers are needed and the active material is etched elsewhere. Secondly the waveguide layer (usually a bulk passive waveguide) is regrown with a high-quality butt-joint.

If required, DBR gratings are patterned on top of the passive waveguide, either using e-beam lithography, or as explained later on, using high resolution ArF lithography. The gratings are etched into a separate grating layer and the full wafer is overgrown with a common top cladding. After overgrowth the wafer is ready for further processing.

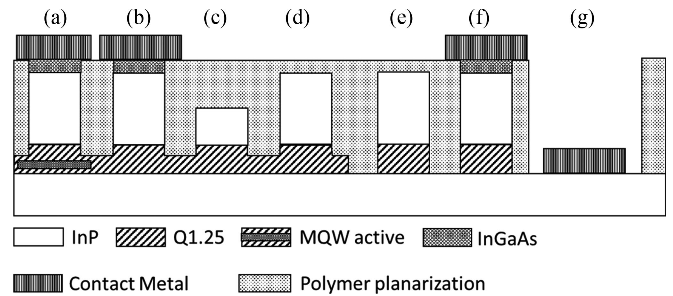

Fig. 2. Schematic representation of the cross sections of the different building blocks. (a)gain/detector/EAM, (b) shallow phase modulator, (c) electrical isolation section, (d) shallow waveguide, (e) deep waveguide, (f) deep phasemodulator, (g) N-contact.

The butt-joint process allows flexible positioning of active elements everywhere in the circuit with a low coupling loss ($\sim$0.1 dB) and low reflections ($<$40 dB) between active and passive elements [6]. By having such low reflections of the butt-joint, the results of the lasers in Section III-B are achievable. This demonstrates the advantage of the InP integration platform.

After epitaxial growth, the waveguides are defined to obtain the different waveguide cross sections as depicted in Fig. 2. All waveguide types are defined in one lithography step to ensure perfect alignment. The waveguides are all etched to their respective depths using an Inductively Coupled Plasma (ICP) dry etch process. This process allows for low surface and sidewall roughness, required for low-loss waveguides.

After etching, all waveguides are passivated with a dielectric layer and on top a Polyimide layer is deposited for planarization to allow a good RF performance of the components. The Polyimide is then etched back and the P- and N-contact metals are applied respectively. After contact metallization an additional interconnect layer is applied.

The wafer is thinned and a backside N-contact is applied. Afterwards the chips are diced and an AR coating is applied.

The flow is designed to allow flexibility and some degree of customization. Fig. 3 shows an overview of the currently available “flavours” of the generic integration process. For different applications, specific optimizations are required. At the moment, up to 3 different materials can be integrated without influencing the performance of the platform. As an example a high speed Receiver is explained: in contrast to the standard process used for MPW, a higher RF performance is required, hence a Semi Insulating (SI) substrate is used. Furthermore, the detectors need to be polarization independent, so a bulk active material is chosen instead of MQW material. The rest of the flow is the same and only at the metallization stage an additional N-contact is introduced and the backside metal is omitted.

B. Building Blocks and PDK

The generic integration platform consists of a number of specific functions that are defined as building blocks. These

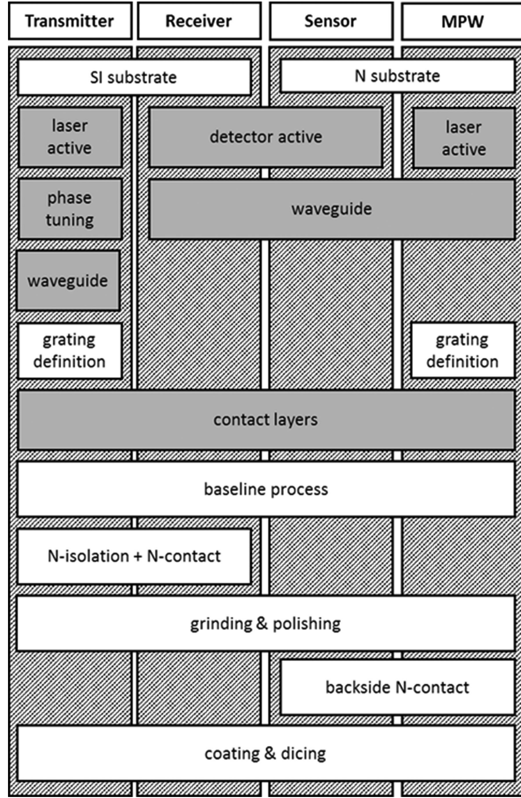

Fig. 3. Schematic overview of the process flow indicating the different flavours or options of the process that are available, optimized for different applications. The epitaxial growth steps are indicated in grey, the processing in white.

building blocks are described in a Process Design Kit, implemented in software. This allows users to design on a functional level and speed up the development cycle. Most building blocks are parameterized and have their own characteristic parameters.

Designers do not have to be concerned about the design of the building block, but they can be taken from a library to build a circuit, and analyze and optimize it with a circuit simulator as explained Section IV.

Because of this, detailed knowledge about the process technology and the layer stacks is no longer required.

This enables the designer to concentrate on a higher abstraction level of circuit design, similar to system designers that use off-the-shelf components. Photonic IC design now is very similar, with the system integrated on a single chip. Furthermore, with respect to system design, the designers can use parameterized building blocks. This allows adaptation of the performance to specific requirements.

Next to the description of the building blocks, the PDK contains a full set of Design Rules to automatically check the design for manufacturability and to flag possible problems in the design.

The basic building blocks and their performance that are available are summarized in Table I. Next to the amplifier that can be used as gain medium for a laser, the electro-optic phase modulator is a key element of the platform. To allow a simple fabrication, the phase modulator in the MPW consists of Q1.25 bulk material and is not optimized for low V_π. The phase modulator can be used in a Mach Zehnder Interferometer

TABLE I
TYPICAL PERFORMANCE PARAMETERS OF BUILDING BLOCKS

Type	Parameter	Typical Performance
Shallow waveguide	Loss	2 dB/cm
Deep waveguide	Loss	3 dB/cm
Curved deep waveguide	Loss	0.1 dB/90°
Crossings	Loss	0.2 dB/crossing
Modefilters	Loss	0.15 dB/modefilter
Shallow-deep transitions	Loss	0.1 dB/transition
SOA	Gain (TE)	26 dB/mm
PIN photodiode	Responsivity (TE)	0.85 A/W
	Polarization dependence	$<$0.3 dB (Receiver or Sensor option)
	Dark current	$<$20 nA
	Bandwidth	$>$20 GHz (SI substrate: Receiver or Transmitter option)
Phase modulator	Bandwidth	9 GHz (N- substrate) $>$20 GHz (SI substrate: Transmitter option)
EAM [28]	Bandwidth	$>$20 GHz (SI substrate)
	Extinction Ration	16 dB (static) 7.7 dB (dynamic)
DBR grating	Coupling coefficient	50 cm^{-1}
1 × 2 MMI	Splitting ratio	0.5
	Loss	1 dB
2 × 2 MMI	Splitting ratio	0.5
	Loss	1 dB

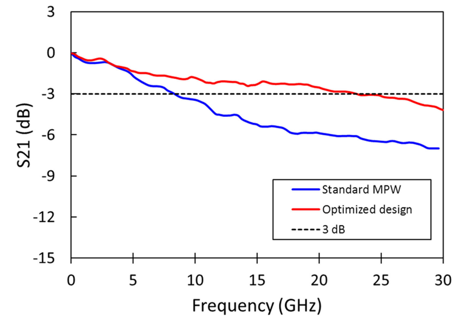

Fig. 4. Electro-optic response of the phase modulator. In blue the standard building block available in the MPW, in red the optimized design on SI substrate for the transmitter.

(MZI) configuration. A typical design consists of phase modulator length of 1.25 mm. The total insertion loss of the MZI is 4 dB, with a V_π of 7.5 V, and DC extinction well above 30 dB. The frequency response of the modulator is shown in Fig. 4. A high frequency design used in the Transmitter is also shown in the same graph. A decrease in V_π to well below 5 V is achieved by using the Quantum Confined Stark Effect in a MQW stack. This is currently being introduced in the Transmitter option.

Apart from the fundamental performance parameters, an important additional parameter to consider for integration is the residual reflection as this might severely influence the performance of the circuit. The reflections of more basic elements are optimized, transitions between different waveguides, butt-joints [6], and crossings [7]. They have reflections well below

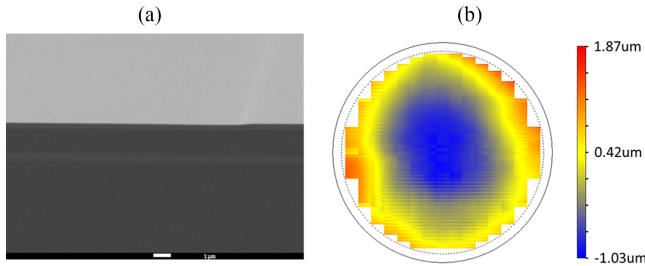

Fig. 5. Wafer flatness after epitaxial active-passive growth. (a) SEM image of the wafer surface (b) Wafer flatness map showing a resulting TTV of 1.4 μm.

-40 dB and close to -50 dB for the crossings. In addition, the Multi Mode Interference (MMI) couplers are optimized to have reflections as low as -34 dB for a 1×2 MMI [8], [9].

C. Optimization and Enhancements

The platform performance is improved by the addition of novel process steps and building blocks. One of the major improvements and the key to high volume manufacturing is the introduction of an ArF based lithography process.

1. High Resolution Lithography: An ASML PAS5500/1100 ArF wafer scanner, adapted to work with 3" and 4" InP substrates is used to develop high resolution lithography for the generic integration platform. To exploit its full capabilities, the wafer flatness is a critical parameter in the ArF lithography. For high resolution lithography, we have to deal with a limited depth of focus of +/− 150 nm. This translates to a strict specification for the wafer flatness. The wafer suppliers have optimized the polishing process and now wafers with a Total Thickness Variation (TTV) close to 2 μm are available. This specification of the substrate quality allows for 100 nm resolution on InP substrates. We have demonstrated exposure of 120 nm spaces on ultraflat InP with a 3σ variation of 10 nm.

For the integration of this lithography in the overall process flow, additional requirements are present. The wafers need to have several epitaxial growth steps as described in the previous paragraph. The epitaxial growth of an active-passive layerstack on Ultra-flat InP Wafers is investigated. Here the main concern is the introduction of "rabbit ears" in the regrowth process: the surface flatness can locally be disturbed by the enhanced growth at the butt-joint. Fig. 5 shows the smooth wafer surface after the regrowth and top cladding growth. From this a limited influence is expected on the total flatness of the wafer. The thickness map, shown in Fig. 5(b) shows the wafer flatness is maintained after growth: the TTV is less than 1.5 μm for the inner dies (with an exclusion zone of 4 mm), which makes these wafers suitable for reliable and reproducible high resolution patterning.

The scanner process is tested on these active-passive wafers. As a demonstrator, deeply etched passive structures are fabricated. The waveguide dimensions are measured over the wafer using a CDSEM (Critical Dimension SEM). The measurements show that a 3σ CD (Critical Dimension) variation of less than 20 nm is obtained over a wafer. This is an improvement of at least a factor of 7 with respect to standard lithography on which we measure a 3σ value of 150 nm. This CD variation is measured after the final waveguide etching. The lithography itself and the etching process contribute approximately equally to this variation.

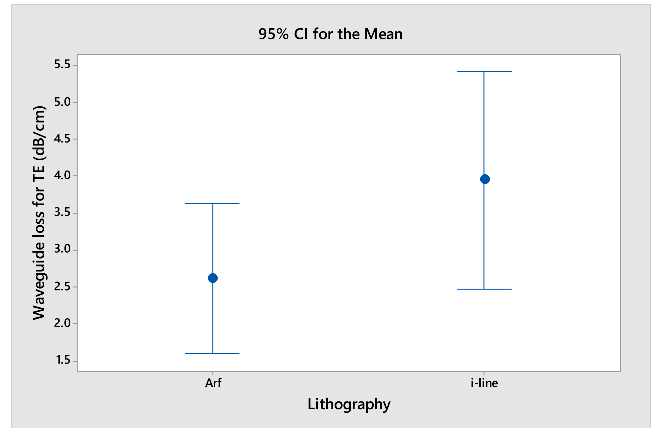

Fig. 6. Losses of deeply etched waveguides patterned using ArF lithography and standard i-line litho. The results are averaged over waveguides with widths varying from 1.3 to 1.7 μm The error bars indicate 95% confidence intervals.

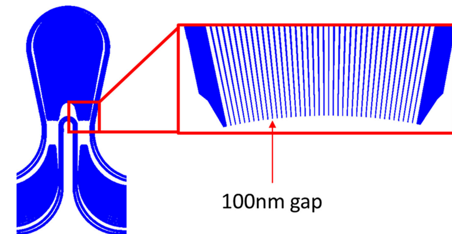

Fig. 7. Mask layout of the high-resolution AWG, the gaps between the waveguides are 100 nm.

The passive losses of waveguides (dominated by the Zn doping from the common top-cladding) produced with the standard process are compared to the scanner process. The losses are measured using a Fabry-Pérot method [10] and the results are plotted in Fig. 6. It is shown that the waveguide losses for the waveguides fabricated with the ArF lithography are as low as 2.5 dB/cm and are as good or better than waveguides produced with i-line lithography. The introduction of the high-resolution lithography does not compromise the losses and this process can be used to fabricate waveguides on the integration platform.

To demonstrate the added value of the high-resolution lithography, we have fabricated Arrayed Waveguide Gratings (AWG). The first devices have been characterised and a large improvement with respect to standard lithography is observed.

The gap between the waveguides at the output of the Free Propagation Region of the AWG is reduced to 100 nm, as shown in Fig. 7. It is expected to reduce the losses dramatically. Furthermore, because of the accurate width definition, it is expected that smaller phase errors are present which will result in lower cross talk levels. In Fig. 8 the measurement results are displayed.

The device is characterised using a tunable laser at one input of the device and the output power at all output ports is measured. The transmission of standard waveguides running along the device, both in- and outside the AWG is measured as a reference for the propagation losses. Currently only the TE polarization

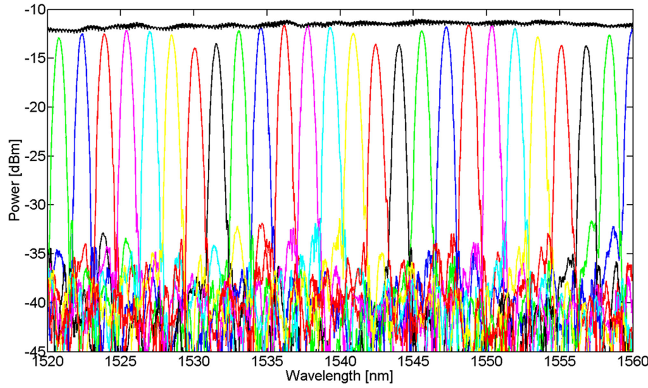

Fig. 8. High resolution AWG output spectrum.

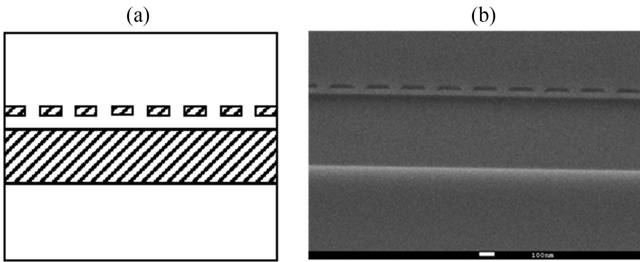

Fig. 9. Cross section of the waveguide showing the gratings (a) Schematic and (b) SEM image.

is regarded. The current design is not optimized for polarization independence. With the better control over the CD, polarization independent design become feasible. This is topic for further investigation. The results are plotted in Fig. 8, the black line in the graphs is the transmission of the standard waveguide.

The insertion losses are close to 0.5 dB and cross talk lower than −25 dB for all channels. This is a huge improvement and will pave the way to densely integrated circuits.

2. DBR Gratings: ArF lithography has successfully been applied to fabricate Distributed Feedback Reflector (DBR) gratings on InP wafers for the first time [11]. The platform operates at wavelengths around 1550 nm, this requires a grating period of about 240 nm, which is below the resolution limit of most conventional lithography techniques. So far, e-beam lithography and holographic lithography have been used to achieve the state-of-the-art performance [12], [13]. However, e-beam lithography has the drawbacks of limited writing area and being time consuming, and holographic lithography is limited to patterning grating features over a large area of the wafer, which limits the design freedom of different wavelength choices over a PIC. ArF lithography combines this freedom of design with a high throughput.

After the waveguide epitaxy, the grating pattern is transferred from the reticle to the photo resist and etched into a hard mask. Then a wet etch is used to etch the materials along the crystal planes. After top layer growth, we obtain the DBR as shown in Fig. 9. The duty cycle is approximately 0.5, which is determined by the layer thicknesses of the grating and spacer layers, the duty cycle of gratings in the hard mask and the crystal plane.

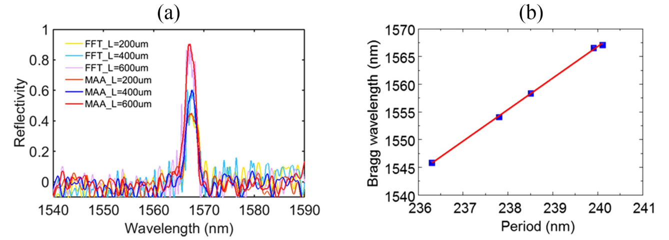

Fig. 10. Experimental results of the DBR gratings. (a) Reflection spectrum (b) Bragg wavelength as a function of grating period.

After the epitaxial process, passive waveguides are fabricated. The lithographical definition of the waveguides is again performed with the ArF scanner to allow a uniform and reproducible width definition over the wafer.

The fabricated DBRs were characterized and compared to the simulations. The influence of the process errors on the device performance was analyzed.

A set of DBRs with periods of 236.3, 237.8, 238.5, 239.9 and 240.1 nm and lengths of 200, 400, 500, and 600 μm are characterized. To enable a fast and self-referenced analysis, the gratings are placed in individual straight waveguides that form a Fabry-Pérot cavity. The reflected power is measured as a function of wavelength. The DBR reflection spectrum is not directly visible in the measurements due to the losses induced by coupling, waveguide propagation and Fabry–Pérot interference. The actual DBR spectrum is extracted using a moving average and filtering out the reflections from the Fabry-Pérot cavity by FFT analysis [14].

The extracted results show the reflection spectra of the DBRs in Fig. 10(a). As expected, it shows that the same grating period results in the same Bragg wavelength and that a longer length of grating results in higher peak reflectivity. The Bragg wavelength of a total of 40 different samples over a wafer has been analyzed. The mean values at 5 periods are shown as blue dots in Fig. 10(b). The Bragg wavelength increases linearly as the period increases, which indicates perfect reproducibility of the lithography process of both the grating and the waveguide width over a large area. The standard deviation of the difference of actual wavelength and the fitted curve is smaller than 0.5 nm, which is sufficient to target the wavelength for tunable DBR gratings.

The results of the passive waveguides, AWGs, and DBR gratings show the feasibility of the ArF scanner for InP based integration. The usage of this tool enables the route to reliable high volume manufacturing.

III. MPW Runs

The generic model brings the technology within reach not only for large companies but also for SMEs and universities. And more importantly it opens the technology for a number of different markets. Because the process is the same for all PICs, their processing can be combined on the same single Multi Project Wafer as shown in Fig. 11. These MPWs offer a large cost advantage for the users, as they all share the cost of a single run. This brings the technology within reach not only for

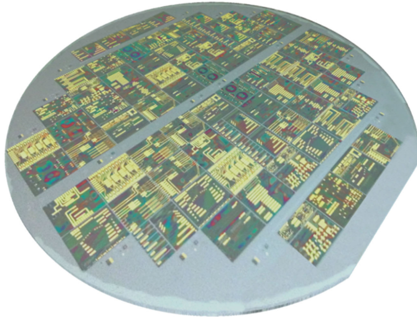

Fig. 11. Multi Project Wafer fabricated using the generic integration process.

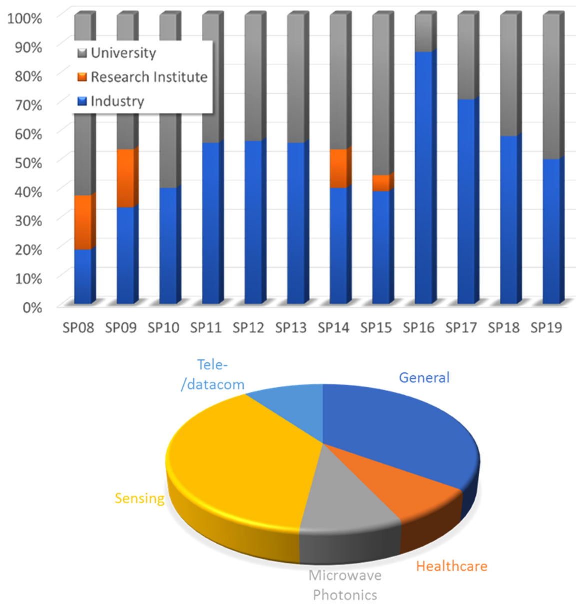

Fig. 12. The percentage of users from academia and industry in the various MPW runs (top) and the application field of the designs (bottom).

large companies but also for SMEs. This has been proven in the commercial MPW runs.

A. MPW Users Analysis

At SMART Photonics only, approximately 200 different designs have been fabricated over the last 3 years. As shown in Fig. 12 the MPW were populated mainly by universities at the start, but now the share of industry is becoming larger. Overall the MPW are a good mix of product development and forward looking research with a fair share for both industry and academia. The bottom graph shows the application fields of the users of the MPW runs for as far as this data is available. This also demonstrates the variety of markets and applications that can profit from this technology.

It is remarkable to note that although the technology has been developed for telecom applications, in the current MPW most of the applications are in different areas such as fiber sensing readouts, gas detection, etc. Furthermore, a number of academic institutes make us of the platform to develop general understanding of the platform capabilities.

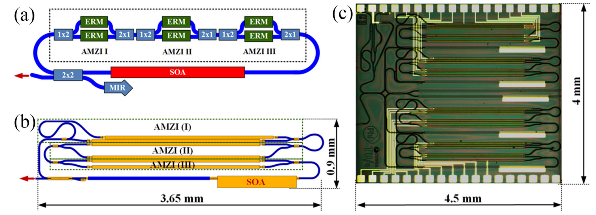

Fig. 13. (a) Schematic diagram and (b) mask layout of the widely tunable laser. (c) Application specific photonic integrated circuit fabricated within a multi project wafer run.

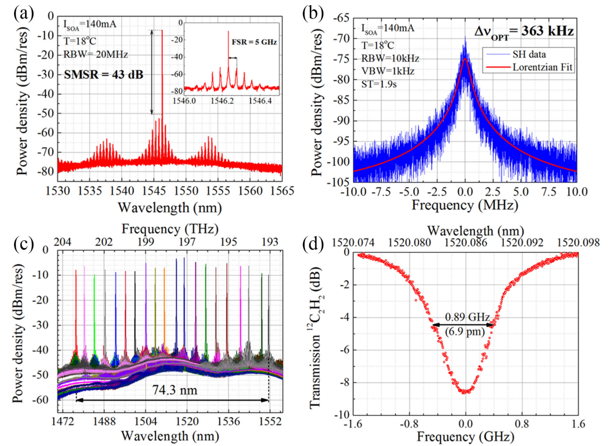

Fig. 14. Typical characteristics of the monolithically integrated tunable laser with AMZI based intracavity filter. (a) Optical spectrum showing single-mode operation of the laser with a detailed view of the lasing mode in the inset. (b) Measured optical linewidth of 363 kHz. (c) Overlapped optical spectra showing a tuning range of 74.3 nm. (d) Fine scan over 0.89 GHz wide absorption line of acetylene.

B. Examples of ASPICs

The wide range of circuits that is possible with the generic platform is demonstrated in this paragraph. Three examples of circuits, fabricated in an MPW are demonstrated.

1) Widely Tunable Monolithically Integrated Laser: A widely tunable laser with a wavelength tuning mechanism based on asymmetric Mach-Zehnder interferometers (AMZI) has been presented [15]. The circuit is based on extended cavity ring laser of which the geometry and corresponding mask layout are shown in. in Fig. 13(a) and (c) respectively.

The laser cavity consists of a semiconductor optical amplifier (SOA), multi-mode interference (MMI) couplers, electro-refractive modulators (ERM) and passive waveguides. All of these components are predefined and standardized building blocks available in foundry's process design kit (PDK). Typical operation characteristics at room temperature are presented in Fig. 14. The laser operates in single mode regime with the optical linewidth measured at 363 kHz. The implemented tuning mechanism is tolerant to fabrication errors and does not require demanding lithography techniques. The fabricated devices have been demonstrated to cover a record tuning range of 74.3 nm in Fig. 14(c). This same tuning mechanism allowed for fine scanning of the laser over a narrow-band absorption line of acetylene in a gas spectroscopy experiment as shown in Fig. 14(d) with resolution of 48 fm (6.3 MHz).

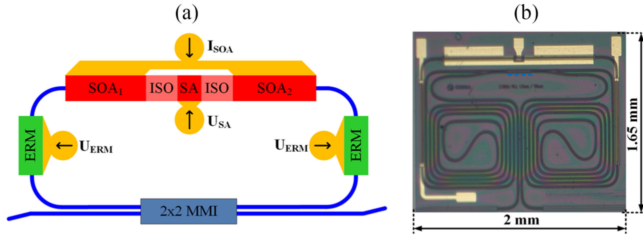

Fig. 15. (a) Schematic diagram of the ring mode-locked laser based on standardized building blocks. (b) A microscope image of the fabricated device with an area of 4 mm^2 (2.3 mm × 1.75 mm).

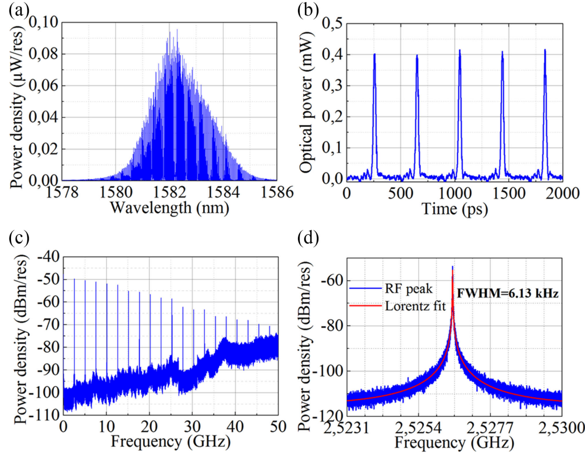

Fig. 16. Output characteristics of the monolithically integrated device operating in a passive mode-locking regime. (a) Optical frequency comb with 3 dB bandwidth of 3 nm. (b) Pulse train measured with an oscilloscope. (d) RF beat signal produced on a fast photodiode. (d) Detailed view of the fundamental frequency beat signal in blue and a weighted Lorentzian fit in red.

An array of four of these independently tunable laser sources combined to a common output has been fabricated within a single 4.5 × 4.0 mm die on a MPW run, as shown on photograph in Fig. 13(c).

2) On-Chip 2.5 GHz Mode-Locked Laser: A monolithic mode-locked ring laser operating at 1.58 μm with a repetition rate of 2.5 GHz has been realized using the active-passive integration technology [16]. The device has been designed for application in a dual-comb Fourier domain spectroscopy system [17]. The cavity of the laser presented schematically in Fig. 15(a) contains two SOAs, a saturable absorbers (SA), electrical isolation (ISO) and passive waveguide sections as well as ERMs to enable fine tuning of the spectral position of the lasing modes. A microscope image of the mode-locked laser with the 3.3 cm long cavity fabricated within an MPW run is shown in Fig. 15(b).

Passive and hybrid mode-locked operation, along with wavelength tuning of the laser modes have been experimentally demonstrated [16], [17]. Typical performance when the laser is operated at room temperature and under DC bias conditions in the passive mode-locking regime is presented in Fig. 16. The laser features a 3 nm wide (−3 dB) optical coherent optical comb, which results in narrow-band (6.13 kHz) electrical beat-tones produced on a high speed photodiode at the frequency corresponding to the fundamental cavity resonance and its harmonics. It forms a train of pulses in the time domain [17].

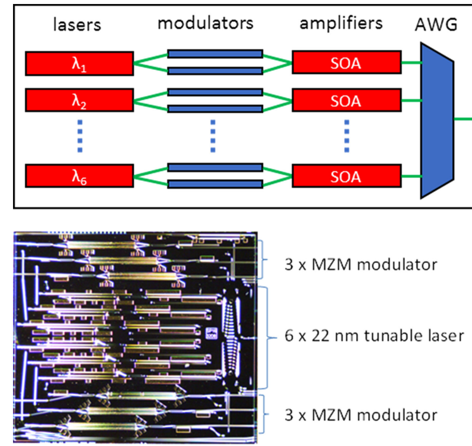

Fig. 17. Schematic principle of operation (top) and a microscope image of the fabricated WDM transmitter with an area of 3.9 × 4.5 mm^2.

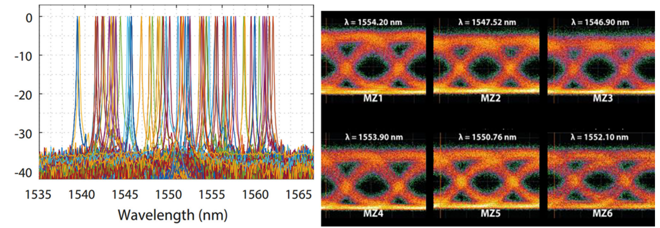

Fig. 18. Tunable laser with 22nm tuning range and the eye diagram measurements at 30 Gb/s OOK modulation.

3) 180 Gbit/s WDM Transmitter: The high density integration capabilities of the platform are demonstrated by the fabrication of an integrated WDM transmitter [18]. The device in Fig. 17 contains 6 channels, connected via 2 AWGs to the output. Each channel consists of a tunable laser, a Mach-Zehnder Interferometer based modulator with Electro-Optic phase modulators in the arms, and a semi-conductor optical amplifier (SOA) to boost the output power. The output multiplexer in Fig. 17 (top) is replaced by two AWGs that are combined using a 1 × 2 MMI coupler to fit the whole device in a standard MPW cell.

The device is designed without using gratings, to reduce processing complexity and achieve lower cost devices. The tunable laser design utilizes a coupled-cavity approach [19], and electro-refractive modulators are using bulk waveguide material to be fully compatible with the standard MPW.

The tunable laser contains a special two-port multi-mode interference reflector as the coupling element and includes a Michelson-Interferometer (MI) as a wavelength selective filter to increase the tuning range [20]. The Vernier-effect between cavity modes is used for mode selection. Fine tuning is performed with phase adjustment sections in the respective cavities.

The distance between adjacent lasers (>150 μm) and modulators (>100 μm) is optimized to reduce electrical and thermal crosstalk effects [21], [22].

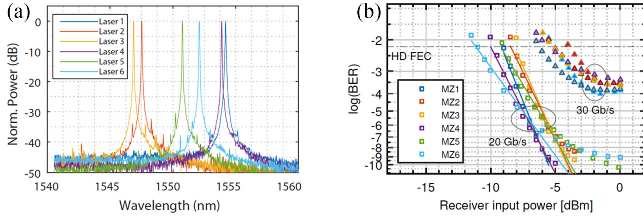

Fig. 19. (a) Wavelength of the laser channels during modulation. (b) Measured BER at 20 Gb/s and 30 Gb/s.

The tuning of the laser is shown in Fig. 18(a), it is demonstrated that the tuning range is 22 nm and the side-mode suppression (SMSR) is >30 dB throughout the whole tuning range.

Large-signal modulation experiments were performed by utilizing the on-chip lasers. The laser wavelengths are tuned to specific wavelengths in order to match with an external AWG bandpass filter that was used in the experimental setup. The optical signal was amplified by an EDFA before entering the receiver and the AWG filter was used to suppress ASE noise. Large-signal modulation eye diagrams are depicted in Fig. 18(b) using a single-drive scheme. Open eyes can be achieved at 30 Gb/s on-off keying in all six channels. The corresponding laser spectra are shown in Fig. 19(a) for the six channels. Good side mode suppression is demonstrated for all channels. The modulated output signal was fed directly to the optical receiver and the eye diagram and BER was measured. Fig. 19(b) shows the BER results and indicates that error-free operation ($<10^{-9}$ BER) at 20 Gb/s is achieved in all six channels. At an increased bitrate of 30 Gb/s, an error-floor is present between 10^{-4} and 10^{-3} BER, indicating that the modulator bandwidth limit is reached. Yet, when utilizing forward error correction techniques error-free operation is possible also at 30 Gb/s. This indicates that the complete transmitter is able to operate at an aggregate capacity of 180 Gb/s with >20 nm tuning range in each channel. Together with the compact size of 17.5 mm^2, the device represents a high capacity density metric of 10 Gb/s/mm^2.

IV. Software and Design Flow

Various software suites provide access to the PDK and an integrated top-down design flow is available supporting the rapid realization of circuits on the platform. VPIphotonics [23] and PhoeniX Software [24] have developed a layout-aware schematic-driven design flow [25], [26] making use of the advanced capabilities of VPIcomponentmaker Photonic Circuits and OptoDesigner. In the PDK parameterized compact models and the required mask layer and layout information is available for use in the circuit simulator and layout tool.. The design flow enables engineers to functionally design the PIC using a comprehensive library of parameterized photonic building blocks. The simulation tool provides a scalable time-and-frequency-domain framework for fast and accurate modeling of large-scale PIC designs [27].

This implementation enables to sweep and optimize parameters in an automated fashion even over layout-related parameters, which enables thorough investigation of sensitivity to fabrication tolerances, and thus, yield analysis for optimal design performance. Orientations and connections of the circuit building blocks are kept and are passed to the mask generation software: PhoeniX Software's OptoDesigner. This way, the layout and intent of the circuit simulation design is kept. The tool uses foundry fabrication data to compile a manufacturable design. The PDK contains this foundry data in form of parameterized photonic building-blocks and an extensive set of design rules. The software makes use of curvilinear design-rule checking features, which is crucial for photonics circuits with numerous bends.

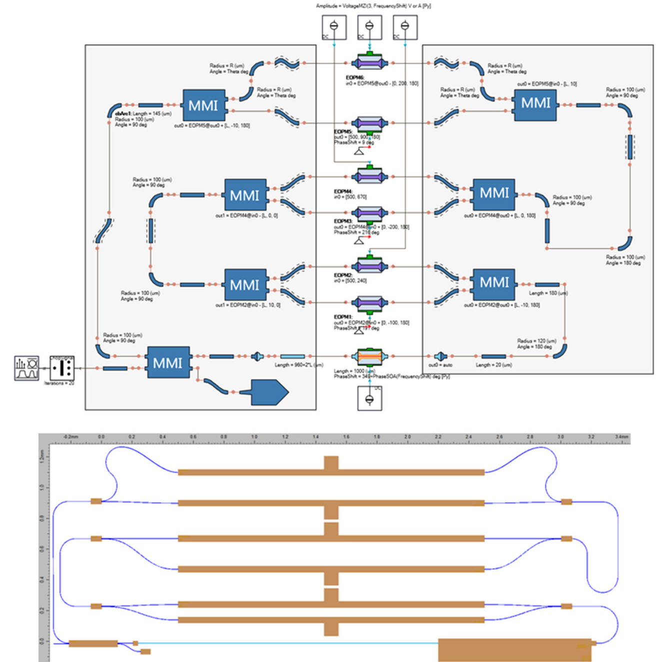

Fig. 20. Simulation setup in VPIcomponentmaker of the widely tunable laser showing all the building blocks and key parameters used (top) and automatically exported layout (bottom) into PhoeniX OptoDesigner.

The design flow is demonstrated by simulating the widely tunable laser described in Section III-B, and depicted in Fig. 13. All the waveguide lengths are important – not only inside each MZI, but also the total length of the whole ring laser cavity. An overview of the implemented design is shown in Fig. 20 After designing MZIs with proper FSRs, matched with the FSR of the whole circuit, and applying estimated voltages to all the phase modulators, one can obtain results as shown in Fig. 21, single-mode lasing at almost any desired wavelength.

These results are in good qualitative agreement with the measured power spectrum in Fig. 14. The simulation suggests the small side-lobes can be further suppressed by careful voltage tuning on the phasemodulators.

The accuracy of the simulation can further be improved by additional verification of the simulation models for the building blocks in the PDK, at the time of writing this is work in progress. This example shows the importance of the layout-aware schematic-driven design approach in which the connections and orientations of the building blocks and their parameters are kept. It allows to design such a circuit with verified functionality in few days.

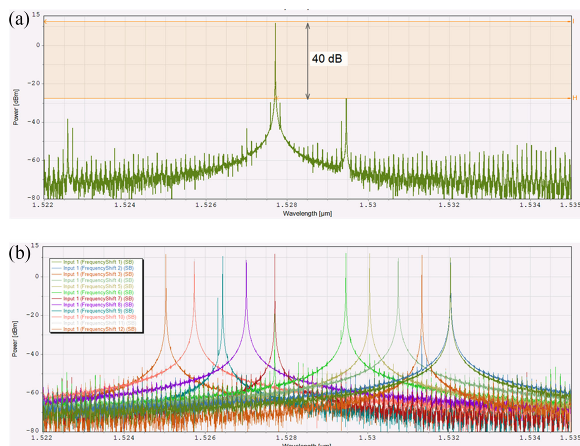

Fig. 21. Simulated laser spectrum of the widely tunable laser (a) and a number of different lasing modes by simulating different phase modulator settings (b). Graphs are generated directly from VPIcomponentmaker.

V. Conclusion

This paper demonstrates the capabilities of the generic integration platform. The large number of designs and the broad application area of the PICs prove the versatile nature of the platform. High density integration is possible and with the current platform capacity densities of 10Gb/mm^2 is achieved. The introduction of high resolution lithography enables reproducible and scalable processes. The combination of low-cost access through MPW runs and the availability of good design tools open up the generic platform for an even broader user base.

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Huub Ambrosius photograph and biography not available at the time of publication.

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