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Layout-Aware Schematic-Driven Design Methodology for Photonic Integrated Circuits

Sergei F. MINGALEEV[1*], Stanislau G. SAVITSKI[1], Eugene S. SOKOLOV[1], Igor G. KOLTCHANOV[2], and André RICHTER[2]
[1]VPI Development Center, Filimonova str. 15, Minsk, 220037, Belarus
[2]VPIphotonics GmbH, Carnotstrasse 6, Berlin, 10587, Germany
[*] sergei.mingaleev@vpiphotonics.com

Impressive advances in integrated Si and InP photonics technologies drive rapid commercialization efforts and raise promises for the rise of an emergent global market. However, costs associated with the design and fabrication of photonic integrated circuits (PICs) are still several orders of magnitude higher than those for their microelectronic counterparts, which limits rapid application of PICs in many areas. The need to reduce these costs has been a major driving force for the integrated photonics development during the past few years. Similar to electronics, the main approach to cost reduction is based on introducing standardized process design kits (PDKs) and a generic foundry model [1-2]. Integration of this approach into modern photonic design automation (PDA) tools is actively expedited, with a focus on interoperability between circuit-level simulators and mask layout design tools [2-5].

Until now, advances in PDA development follow the historic development of electronic design automation (EDA) tools, adding support of schematic-driven layout [4-5] and layout versus schematic (LVS) [5] design methodologies. In application to integrated photonics, however, interferences of optical signals play a major role and consequently the lengths of optical connectors cannot be ignored even in the first approximation. Therefore, such a design flow leads to very frequent iterations between separate phases of schematic capture, waveguide routing, design rule checking (DRC), and LVS verification, clearly playing against demanding time-to-market requirements. Attempts to resolve similar problems in designing high-frequency analogue electronics initiated the development of novel parasitic- and layout-aware circuit design approaches [6], leading to much closer integration between circuit and layout EDA tools.

We introduce here a novel layout-aware schematic-driven PIC design methodology: a circuit-level simulator supports the capability to specify directly physical locations and orientations of PDK building blocks (BBs) on the final layout (when required by DRC and packaging specifications or layout optimization) and to connect sub-circuits having fixed locations by smart elastic optical connectors. This allows combining graphical schematic capture and automated waveguide routing, which are currently considered separately representing a major problem for PIC designers. Key enabler for this functionality is the seamless integration of circuit and layout tools: a circuit simulator automatically and invisibly for users invokes a layout design tool to determine the actual physical lengths and shapes of all elastic connectors, constructs compact simulation models for them, and after that initiates the circuit simulations (see Fig. 1, top).

We implemented this design methodology by combining VPIcomponentMaker Photonic Circuits [7] and PhoeniX OptoDesigner [8] (see Fig. 1, bottom). Our solution supports hierarchical designs and advanced parameter scripting [4], realizing a fast and user-friendly design flow for large-scale PICs. Importantly, parameter sweep and circuit

optimization, sensitivity and yield analysis are supported transparently for PIC designers allowing them to greatly increase their overall productivity.

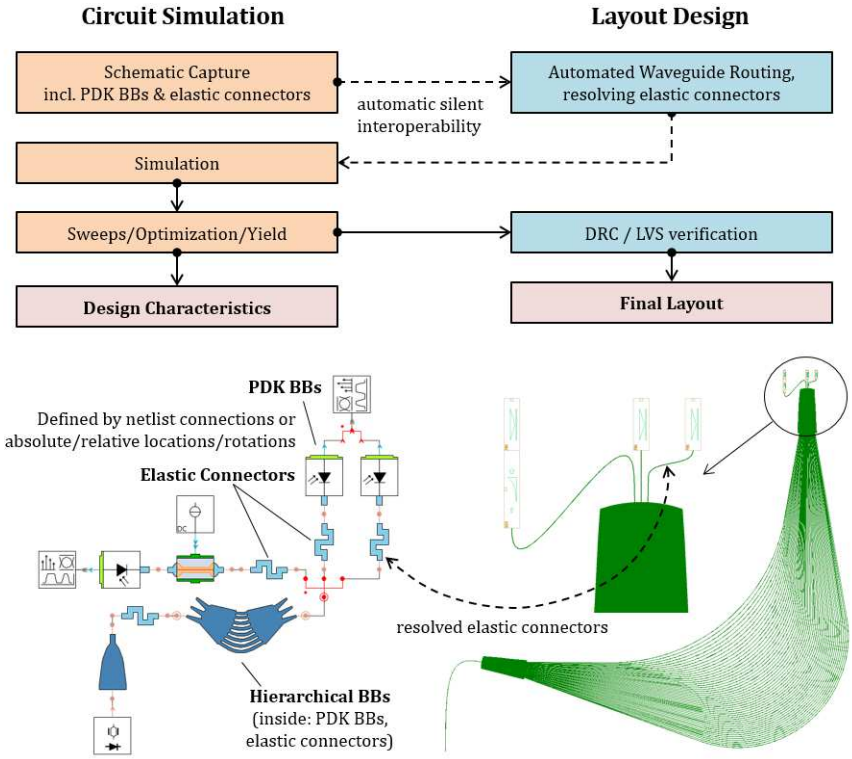

Fig. 52. Layout-aware schematic-driven design methodology and its implementation with VPIcomponentMaker Photonic Circuits and PhoeniX OptoDesigner.

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